

Digital Logic Circuits Volume III

An Online Continuing Education Course for Engineers

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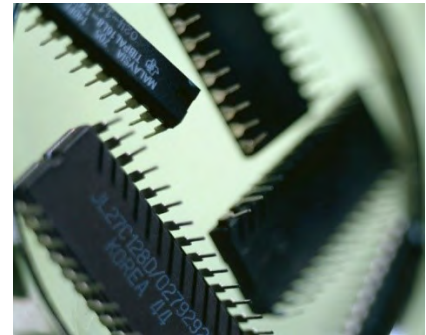
Credit: 4 Hours / 4 PDH / 4 CPD

Digital Logic Circuits Volume III

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Introduction

This is the third course in a series of three courses on digital logic circuits. In Digital Logic Circuits, Volume II, Fundamental Logic Circuits, we studied the four basic logic gates that make up the foundation for digital equipment and looked at the types of logic that are used in equipment to accomplish the desired results.



Digital equipment must be capable of many more operations than those described in volume II of this series. Provisions must be made for accepting information; performing arithmetic or logic operations; and transferring, storing, and outputting information. Timing circuits are included to ensure that all operations occur at the proper time.

In this course we will study the logic circuits used to perform the operations mentioned above. This includes Exclusive OR/NOR Gates, adders, flip-flop circuits, clocks, counters and registers. The first chapter explains the operation of the Exclusive OR gates and the Exclusive NOR gates in detail.

Chapter 1: The Exclusive OR/NOR Gate

The *exclusive OR gate* is a modified OR gate that produces a HIGH output when only one of the inputs is HIGH. You will often see the abbreviation X-OR used to identify this gate. When both inputs are HIGH or when both inputs are LOW, the output is LOW.

The standard symbol for an exclusive OR gate is shown in Figure 1 along with the associated Truth Table in Figure 2. The operation function sign for the exclusive OR gate is \oplus .

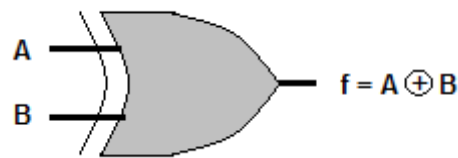


Figure 1

Truth Table		
A	B	f
0	0	0
0	1	1
1	0	1
1	1	0

Figure 2

If you were to observe the input and output signals of an X-OR gate, the results would be similar to those shown in Figure 3. At T_0 , both inputs are LOW and the output is LOW. At T_1 , A goes to HIGH and remains HIGH until T_2 . During this time the output is HIGH. At T_3 , B goes HIGH and remains HIGH through T_5 . At T_4 , A again goes HIGH and remains HIGH through T_5 . Between T_3 and T_4 , the output is HIGH. At T_4 , when both A and B are HIGH, the output goes LOW.

Timing Diagram

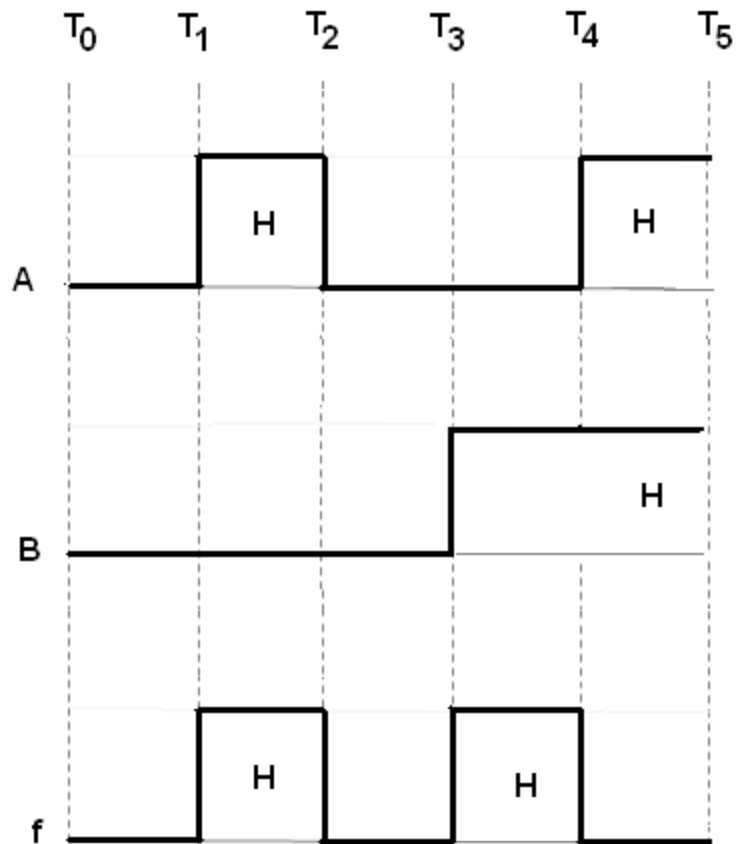


Figure 3

The Exclusive NOR Gate

The exclusive NOR (X-NOR) gate is nothing more than an X-OR gate with an inverted output. It produces a HIGH output when the inputs are either all HIGH or all LOW. The standard symbol and the Truth Table are shown in Figure 4. The operation function sign is \oplus with a vinculum over the entire expression.

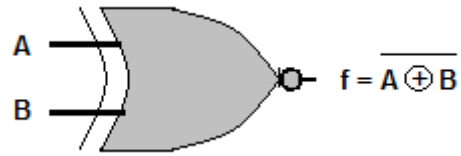


Figure 4

Truth Table		
A	B	F
0	0	1
0	1	0
1	0	0
1	1	1

A timing diagram for the X-NOR gate is shown in Figure 5. You can see that from T_0 to T_1 , when both inputs are LOW, the output is HIGH. The output goes LOW when the inputs are opposite; one HIGH and the other LOW. At time T_3 , both inputs go HIGH causing the output to go HIGH.

Timing Diagram

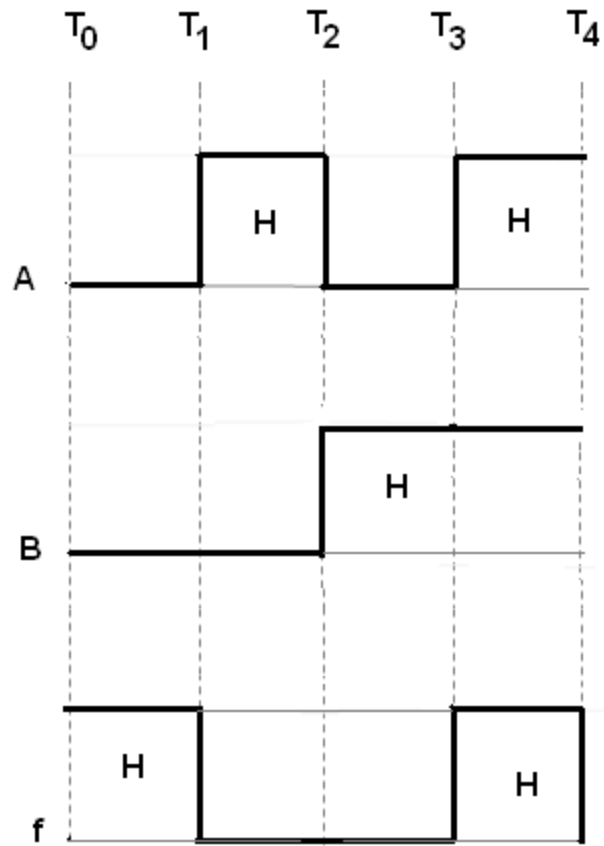


Figure 5

Chapter 2: Adders

Adders are combinations of logic gates that combine binary values to obtain a sum. They are classified according to their ability to accept and combine the digits. In this section we will discuss quarter adders, half adders, and full adders.

Quarter Adder

A *quarter adder* is a circuit that can add two binary digits but will not produce a carry. This circuit will produce the following results:

0 plus 0 = 0

0 plus 1 = 1

1 plus 0 = 1

1 plus 1 = 0 (no carry)

You will notice that the output of the OR gate is HIGH (1) when either input is HIGH (1). Therefore, an X-OR gate produces a HIGH (1) when either input is HIGH (1) or when both inputs are LOW (0).

The combination of gates that produces the sum of two bits is shown in Figure 2-1. When A and B are both LOW (0), the output of the OR gate is LOW (0). When A is HIGH (1) and B is LOW (0), the output of the OR gate is HIGH (1). When A is LOW (0) and B is HIGH (1), the output of the OR gate is HIGH (1). When both A and B are HIGH (1), the output of the OR gate is HIGH (1). The output of the X-OR gate is LOW (0) when both inputs are the same (both LOW or both HIGH) and the output of the X-OR gate is HIGH (1) when the inputs are different (one LOW and one HIGH).



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the Truth Table of an X-

ts. When A and B are both LOW (0), the output of the OR gate is LOW (0). When A is HIGH (1) and B is LOW (0), the output of the OR gate is HIGH (1). When A is LOW (0) and B is HIGH (1), the output of the OR gate is HIGH (1). When both A and B are HIGH (1), the output of the OR gate is HIGH (1). The output of the X-OR gate is LOW (0) when both inputs are the same (both LOW or both HIGH) and the output of the X-OR gate is HIGH (1) when the inputs are different (one LOW and one HIGH).